Micro-Power Data Converters

Gabor C. Temes

School of EECS
Oregon State University

December 2012
Outline

- Micro-power D/A converters:
  - Overview of CMOS DACs
  - Switched-capacitor DACs
  - Quasi-passive two-C DAC
  - Quasi-passive pipeline DAC
  - Delta-sigma DACs.

- Micro-power A/D converters:
  - Overview of CMOS ADCs
  - SAR ADC, pipeline SAR ADC
  - Multiplexed incremental ADC
  - Extended-count hybrid ADC.
Applications

- Battery-powered or scavenging medical devices (hearing aids, ECG, EEG, etc. sensors, brain stimulators);
- Wireless sensor networks for industrial and environmental applications;
- Imagers;
- RFID systems.

Typical target specifications:

DACs: BW up to 20 kHz, ENOB 14 - 15 bits, 20-bit input;

ADCs: BW = up to 5 kHz; ENOB > 12 bits; power < 5 microwatts; input signal amplitude 0.1 ~ 5 mV.
Power Saving in Data Converters

- Stages: S/Hs, buffers, comparators, SC blocks.
- S/H: whenever possible, use passive (SC) circuitry; if not, use direct charge transfer (DCT) amplifier stage.
- Buffers: use DCT stage.
- Comparators: use dynamic circuitry.
- SC circuits: use minimally busy circuitry. Reduce dynamic power dissipation.
- Transistor circuits: consider weak inversion operation.
- Logic: consider asynchronous or semi-synchronous switching.
- Use low-power digitally corrected analog circuits.
Classification of DACs

• “Nyquist-rate” DAC: “data converter”, memoryless, one-to-one correspondence between each input digital word and the corresponding output analog sample;

• “Oversampled” DAC: “signal converter”, has memory (finite or infinite length), so digital output depends on all previous inputs and outputs.

• Sampling rates may not be very different between the two.
### Classification of Nyquist-rate D/A converters

Classification of Nyquist-rate D/A converters

\( T = \) clock period, \( N = \) resolution in bits

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Conversion time</th>
<th>Latency (delay)</th>
<th>Resolution (typical)</th>
<th>Usual implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallel (flash)</td>
<td>( T )</td>
<td>( T )</td>
<td>5-12 bits</td>
<td>Current steering; voltage division; charge sharing</td>
</tr>
<tr>
<td>Pipeline</td>
<td>( T )</td>
<td>( NT )</td>
<td>8-12 bits</td>
<td>Passive SC; active (opamp) stages</td>
</tr>
<tr>
<td>Serial</td>
<td>( NT )</td>
<td>( NT )</td>
<td>8-12 bits</td>
<td>2-capacitor SC stage</td>
</tr>
<tr>
<td>Counting</td>
<td>( 2^{NT} )</td>
<td>( 2^{NT} )</td>
<td>15-22 bits</td>
<td>SC integrator + digital comparator</td>
</tr>
</tbody>
</table>
Nyquist-Rate DACs

- Parallel (flash) DACs: conversion time and latency is $T$; resolution $N < 10$ bits; implementation R-string or R-2R ladder, current sources, switched-capacitor (SC) stage. Hybrid R + SC also practical.

- Pipelined DACs: conversion time $T$; latency $NT$; $N < 12$ bits; SC stages.

- Serial DACs: conversion time and latency $NT$; $N < 12$ bits; 2-C stages.

- Counting DAC: conversion time and latency = $2^N \cdot T$; $N < 24$ bits; SC or RC integrators.
Oversampled CMOS DACs

- Nyquist-rate vs. oversampled DACs: in oversampled DAC, the word length can be reduced to 1 ~ 5 bits.

- Mismatch errors can be suppressed in signal band using dynamic element matching.

- High accuracy can be obtained with simple low-power analog circuitry, but complex digital delta-sigma loop and prefilter may be required.

- May only be economical in fine-line process, for high-resolution low-power DAC applications.
Nyquist-Rate Parallel DACs

- R-string or R-2R ladder: large area, large mismatch errors, static dissipation – seldom practical in low-power applications.

- Current-source DAC: large mismatch error, static dissipation – seldom used in slow low-power DACs.

- SC stages: binary-weighted or unary (unit-element-based) charge redistribution circuits. Unary is more complex, but the glitches are reduced, the conversion monotonicity is guaranteed, and dynamic element matching (DEM) may be possible.
Unary SC DAC Stage

- Unary SC DAC: monotonic, low glitch. May use DEM.
Binary SC DAC Stage

- Non-monotonic, large glitch. No DEM.

- Both circuits use correlated double sampling for amplifier offset cancellation and for gain boosting.
SC DAC Using DCT Circuit

- Direct charge transfer (DCT) reduces the slewing and settling requirements on the amplifier, since it need not provide current to the feedback branch:
Two-Capacitor DAC

- Simple, low-power and fast, but mismatch introduces large spurs.
- Digital dither, correction or mismatch shaping possible.
- Serial DAC; needs $N$ clock periods for $N$-bit resolution.
- May be time interleaved or pipelined for Nyquist-rate operation.

![Two-Capacitor DAC Circuit Diagram](image)
Quasi-Passive Cyclic DAC

- Operation for \(x(n) = 1, 0, 1, 1\):
  - Charge redistribution between two equal-valued capacitors
  - Serial digital input; LSB first
  - \(\Phi_1\) and \(\Phi_2\) are two non-overlapping clock phases
  - Conversion follows equation

\[
V_{\text{out}} = V_{\text{ref}} \sum_{i=1}^{N} b_i 2^{-i}
\]

Capacitor Mismatch

- Capacitor mismatch effects (radix mismatch):
  - Conversion accuracy limited by capacitor matching accuracy;
  - Capacitor mismatch introduces nonlinearity;
  - Plots show performance degradation (bottom) in SNDR and SFDR compared with ideal matching (top).
Mismatch Compensation (1)

• Switching techniques:
  – Compensative switching
    • The roles of the two capacitor is interchangeable
    • The roles of the capacitors can be chosen for every bit
    • An algorithm was developed to minimize the conversion error for any digital word [2]
    • The switching pattern is input dependent
    • First-order error canceled for 31% of the input codes; reduced to 1/10 for 48% of the input codes.

Mismatch Compensation (2)

- Switching techniques:
  - Complementary switching:
    - Digital word fed to DAC twice; once with normal arrangement, once with swapped roles of $C_1$ and $C_2$
    - Outputs of the two conversions are added (or averaged), actively or passively;
    - First-order mismatch compensation, at cost of doubled conversion time.

Mismatch Compensation (3)

- Switching techniques:
  - Input-word-splitting compensative switching
    - Compensative switching [2] does not compensate for all input codes
    - Split digital input into sum of two digital codes
    - The conversion errors reduced using compensative switching for the two new digital inputs
    - Final output is the sum of the two conversions
    - Needs two sets of 2-C DACs
    - Needs analog summation
    - Needs sophisticated algorithm for splitting the input word

Mismatch Compensation (4)

• Switching techniques

  – Alternately complementary switching
    • Roles of $C_1$ and $C_2$ are swapped alternately in the first cycle and adopt complementary switching [3] for the second conversion cycle
    • Output of the two conversions are summed (or averaged)
    • INL improved due to cancellation of major second-order error

  – Hybrid switching
    • Averaging conversion results of complementary switching and alternately complementary switching
    • Smaller INL; fourfold conversion cycles

Mismatch Compensation (5)

- Mismatch shaping using oversampling $\Delta\Sigma$ modulator:
  - Digital state machine to control switching sequence of a symmetric two-capacitor DAC
  - Improved linearity; better shaping for higher OSR
  - Needs $2N$ clock cycles for $N$-bit D/A


Simulated (FFT) performance of the DAC without (a) and with (b) mismatch shaping using a second-order loop filter
Mismatch Compensation (6)

- **Radix-Based Digital Correction**
  - Compensation in digital domain
    - Effectively a radix-\((C_1/C_2)\) conversion
    \[
    V_{\text{out}} = V_{\text{ref}} \left(\frac{C_1}{C_2}\right) \sum_{i=1}^{N} b_i \left(1 + \frac{C_1}{C_2}\right)^{-1}
    \]
    - Assumes known mismatch \(2(C_1-C_2)/(C_1+C_2)\), or \(C_1/C_2\)
    - ADC-like algorithm predistorts digital input
    - Feeds predistorted digital words into the 2-C DAC
    - Better performance when DAC resolution is high
    - Needs value of mismatch, with high accuracy.

- J. Cao et al., ISCAS 2010
Two-Capacitor DAC Variations

• Time interleaved 2-C DAC
  – Time interleaving 2-C blocks improves throughput speed
  – Capacitor mismatch between channels is tolerable
  – Direct-charge-transfer buffer reduces power consumption

• Pipelined quasi-passive cyclic DAC
  – Same operation as 2-C DAC
  – Information passed on to the last capacitor and DCT output buffer

Quasi-Passive SC Pipeline DAC

- Serial digital input, Nyquist-rate output;
- Tolerant to switch nonidealities; little glitching;
- Capacitor mismatches, DCT buffer errors limit operation to 11 – 12 bit accuracy.
SC Pipeline DAC

- Pipelined version of the two-C DAC.
- Bits are entered serially, starting with LSB controlling the charging of C₁.
- Charges are shared between adjacent capacitors, rippling down the pipeline.
- After delivering charge, each C is free to receive new one.
- Three clock phases are needed.
- Last C voltage is buffered and read out.
Segmented SC Pipeline DAC

- For high accuracy, the pipeline DAC may be combined with a unary MSB DAC, and use dynamic element matching (DEM).
- Unary DAC with DCT buffer:
Segmented DAC Realization

• Example of 6-bit DAC with 4+2 segmentation.

• For $N$ bits, it requires $(n_{\text{LSB}}+1)+(2^{n_{\text{MSB}}}-1)$ equal valued capacitors, where $N = n_{\text{LSB}} + n_{\text{MSB}}$. 
Dynamic Element Matching (DEM)

- Multi-Segmented Quasi-Passive Pipeline DAC (7+4+4). 0.1% error.
- Response on the left is without DWA, and on the right is with DWA.

Fig. DWA Effect
**ΔΣ DAC Structure**

Block diagram of a ΔΣ DAC.

- **IF**: Interpolation Filter
- **NL**: Noise-shaping Loop
- **DAC**: Digital-Analog Converter
- **LPF**: Lowpass Filter

Single-bit DAC can be linear. For a few bits (2-4), DEM can be used.

Signal and noise spectra in a ΔΣ DAC.
ΔΣ DAC Examples

Combined DAC, DCT and filter for a multi-bit ΔΣ DAC [8].

Another ΔΣ DAC with merged DAC, DCT and SCF filter functions [15].
Micro-Power Delta-Sigma DACs

- Digital interpolation filter is followed by digital D-S loop, and a DCT stage performing D/A conversion and pre-filtering.
- Low-resolution SC DAC can be simple, low power.
- Easy trade-off between speed, accuracy and power dissipation.
- Passive R-C reconstruction filter may be possible.
Classification of ADCs

• “Nyquist-rate” ADCs: sample-by-sample memoryless conversion. May use memory in period between samples, but not beyond. “Data converters”.

• “Oversampled” ADCs: each output word depends on all earlier input values. Memory-assisted conversion [2]. “Signal converters”.

• Generally, the Nyquist-rate converters are designed in the time domain, oversampled ones in the frequency domain.
## Classification of Nyquist-rate ADCs

\((T=\text{clock period}, \, N=\text{resolution in bits})\)

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Conversion time</th>
<th>Latency (delay)</th>
<th>Resolution (typical)</th>
<th>Usual implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallel (flash)</td>
<td>(T)</td>
<td>(T)</td>
<td>5-9 bits</td>
<td>R string, comparators</td>
</tr>
<tr>
<td>Pipeline</td>
<td>(T)</td>
<td>(NT)</td>
<td>10-14 bits</td>
<td>SC stages+ T/H+ opamps.</td>
</tr>
<tr>
<td>Subranging (half-flash)</td>
<td>(2T)</td>
<td>(2T)</td>
<td>8-12 bits</td>
<td>R strings, comparators</td>
</tr>
<tr>
<td>Serial (Succ.appr)</td>
<td>(NT)</td>
<td>(NT)</td>
<td>7-12 bits</td>
<td>SC charge redistribution</td>
</tr>
<tr>
<td>Counting</td>
<td>(2^NT)</td>
<td>(2^NT)</td>
<td>16-24 bits</td>
<td>SC or CT integrator</td>
</tr>
</tbody>
</table>

---

Incremental ADCs

- *Nyquist-rate ADC*, but it finds each sample using a memoried oversampled converter.

- After an input sample was converted, all internal memories are reset before the next input is entered.

- Can combine the high accuracy of oversampled ADC with the flexibility of the Nyquist–rate ADC for multiplexing, sleep cycles, etc. Simple digital post processing needed. Low power possible.
Micro-Power ADCs

• Micro power: minimum number of active devices, no static power dissipation.

• Favorites: successive-approximation register (SAR) ADCs, incremental and extended-counting ADCs (IDCs and ECCs).

• SAR ADCs can provide up to about 12 bits at several MS/s with a few μW dissipation. IADCs can provide up to 22 bits, with kS/s BW and a few μW.
Successive-Approximation-Register ADC

- Serial divided-reference operation: \( N + 1 \) or \( N + 2 \) cycles for \( N \)-bit resolution;
- DAC and comparator errors limit the accuracy;
- Needs S/H. (It may be part of the DAC.)
- For low speeds, the active blocks dissipate most of the power.
Conventional SAR ADC [7],[8]

- Conventional SAR ADC (3 bits) operation:
  1. Store $Vin$; shift level of top node voltage $V$ to $-Vin$;
  2. Raise $V$ by $V_{ref}/2$; compare with $Vin$; get MSB.
  3. Keep $V$ or return it to $-Vin$;
  4. Repeat for all bits.

$$E_{total} = \frac{49}{8} CV_{ref}^2$$
Conventional SAR ADC

• Advantages: simple logic, low static power dissipation, large capacitances switched first, hence low $kT/C$ noise.

• Drawbacks: large capacitance spread, large chip area, large dynamic power loss for $N > 8$.

• Capacitance spread may be reduced by using split DAC array, or C-2C ladder. These are however more parasitic and element–value sensitive circuits.
Energy Loss in SAR C Arrays

- Energy required to charge an uncharged capacitor $C$ to voltage $V$ is $E = C.V^2$. Half is lost in the switch.

- In SAR ADC, for $Vin = 0$ the initial step draws an energy $2^{N-2}CV_{ref}^2$ Joules, and subsequent steps draw comparable amounts from $V_{ref}$.

- Worst case is $Vin \sim 0$. Total dynamic power loss is then $P \sim [2^N/1.2] f.C.V_{ref}^2$. This may be significant. (For $N = 10$, $C = 50$ fF, $V_{ref} = 1$ V, $f = 1$ MHz, $P \sim 43$ uW.) Using a modified DAC circuit, e.g., junction splitting SAR, can reduce the power to $P = f.C.V_{ref}^2$. 
Semi-Synchronous SAR ADC

- SAR ADC normally designed for worst-case comparator decision time and accurate DAC settling.

- In reality, one or the other conditions is not needed.

Semi-Synchronous SAR ADC

- Required times:
Semi-Synchronous SAR ADC

- After a “hard” decision, inaccurate DAC settling is OK.
INL and DNL Performance

![Graph showing INL and DNL Performance](image)
Simpler SAR ADC Circuit

- Conventional implementation needs $2^N$ unit capacitors. Reduced cap implementation (W. Yu et al., ISCAS 2010):

![SAR ADC Circuit Diagram]

Needs $2^N$ clock periods for every output word.
Simpler SAR ADC

- Four capacitors and a charge copier can generate all voltages for the SAR ADC.

- In each period, an upper limit, a lower limit and their average value are developed.

- The active block acts as a charge copier during $\Phi_1 = 1$, and as a comparator during $\Phi_2 = 1$.

- Active block needs more power than in other SAR ADCs.
Faster SAR ADC Circuit [9]

- Faster implementation.
- Large spread of capacitors and/or voltages. May be remedied.
Faster SAR ADC

• Input capacitor is charged to $V_{in}$, and then the other capacitors add or subtract charges scaled from $C.V_r$ as controlled by the comparator output bits.

• The voltages are divided by 2 in each step.

• Also possible to use scaled capacitors and unscaled voltages, or scale both $C$ and $V$.

• Concept shown only.
Junction-Splitting SAR [8]

3-bit junction-splitting SAR ADC. $V_{out}$ is determined by the ratio of the capacitances, not by their absolute values.

All blocks are appended to the capacitor array one-by-one, to generate the desired output voltage.

Total capacitance: $2^N \cdot C$, where C is the unit capacitance.

- The power consumption for $V_{in}=0$ is now only $f \cdot V_{ref}^2 \cdot C \cdot \left(1 - \frac{1}{2^N}\right)$
- Smallest caps produce MSBs. Reduced accuracy, more noise!

Pipeline SAR ADC

- Provides an output word in each clock period – faster.
- Uses passive SC S/Hs and tapered DACs – low power.

Simulation Results

- All switches in the sampling parts are real. Sampling frequency is 1GHz.

SNR = 39.8dB
Junction-Splitting Pipelined SAR ADC

For 8-bit SAR ADC:

**Conventional**

- 256 C, 1X speed, 1X power consumption

**Junction splitting**

- 256 C, 1X speed, 0.25X power consumption

**Junction-Splitting pipeline**

- 512 C, 8X speed, 2X power consumption

* J. Lin, W. Yu and G. C. Temes, “Micro-power time-interleaved and pipelined SAR ADCs,” ISCAS 2010
Two-Step Split-Junction SAR ADC

For a 6-bit SAR

first 3 bits (MSB)
coarse quantization, the same as split-junction SAR

last 3 bits (LSB)
fine quantization, interpolate with DAC1 and DAC2

Saves 90% of capacitor area and power consumption.

Power Consumption vs. Output Digital Code

- Conventional SAR ADC
- Conventional Pipelined SAR ADC
- Junction-Splitting/Segmented Pipelined SAR ADC
- Hybrid SAR ADC

Normalized Switching Energy vs. Output Digital Code

- Avg. of Conv. SAR ADC
- Avg. of Conv. Pipelined SAR ADC
- Avg. of J.S./Segm. Pipelined SAR ADC
- Avg. of Hybrid SAR ADC
## Comparison of Different SAR ADCs

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Throughput (word/period)</th>
<th>$P_{\text{Dynamic}/CV_{\text{ref}}^2}$ for code 00...0</th>
<th>Total Capacitance</th>
<th>Number of Switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conv. Single SAR ADC</td>
<td>1/N</td>
<td>$\frac{5}{6} \cdot 2^N - \frac{1}{2} \cdot 2^{-N} - 1$</td>
<td>$2^N \cdot C$</td>
<td>$2 \cdot (N + 1)$</td>
</tr>
<tr>
<td>Energy-efficient Single SAR ADC</td>
<td>1/N</td>
<td>$1 - 2^{-N}$</td>
<td>$2^N \cdot C$</td>
<td>$3 \cdot N - 1$</td>
</tr>
<tr>
<td>Conv. T.I. SAR ADC</td>
<td>1</td>
<td>$\frac{5}{6} \cdot 2^N - \frac{1}{2} \cdot 2^{-N} - 1$</td>
<td>$N \cdot 2^N \cdot C$</td>
<td>$2 \cdot N \cdot (N + 1)$</td>
</tr>
<tr>
<td>T.I. Segmented SAR ADC</td>
<td>1</td>
<td>$1 - 2^{-N}$</td>
<td>$(2^{N+1} - 2) \cdot C$</td>
<td>$\frac{1}{3} N^3 + N^2 + \frac{2}{3} N$</td>
</tr>
<tr>
<td>Conv. Pipelined SAR ADC</td>
<td>1</td>
<td>$N - 1 + 2^{-N}$</td>
<td>$(2^{N+1} - 2) \cdot C$</td>
<td>$\frac{1}{2} N^2 + \frac{1}{2} N - 1$</td>
</tr>
<tr>
<td>Segmented Pipelined SAR ADC</td>
<td>1</td>
<td>$1 - 2^{-N}$</td>
<td>$(2^{N+1} - 2) \cdot C$</td>
<td>$\frac{1}{3} N^3 + 2N^2 + \frac{2}{3} N$</td>
</tr>
<tr>
<td>Two-step (hybrid) SAR ADC</td>
<td>1/(N+1)</td>
<td>$1 - 2^{-\frac{N}{2}}$ N is an even.</td>
<td>$2^{\frac{N+1}{2}} \cdot C$ N is an even.</td>
<td>$\frac{1}{4} N^2 + \frac{7}{2} N + 1$ N is an even.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$1 - 2^{-\frac{N+1}{2}}$ N is an odd.</td>
<td>$2^{\frac{N+1}{2}} \cdot C$ N is an odd.</td>
<td>$\frac{1}{4} N^2 + 4N + \frac{19}{4}$ N is an odd.</td>
</tr>
</tbody>
</table>
ADC Architectures

Delta-Sigma ($\Delta\Sigma$) Modulators

\[ STF(z) = z^{-1} \]
\[ NTF(z) = 1 - z^{-1} \]

Incremental ADCs: \( \Delta \Sigma \) ADCs which are reset after each conversion. Properties:

- Flexible trade-off between OSR and power dissipation;
- Limited memory – stable and not tonal;
- Well suited for instrumentation and measurement (I&M) applications;
- High absolute accuracy possible;
- Allows for accurate gain and offset error correction;
- Easily multiplexed, or operated intermittently.
- Decimation filter simpler, easily optimized for SNR. Low latency!
Incremental ADC - Publications

• First incremental ADC (bipolar, 17-bit resolution, first-order ΔΣ loop)

• Further research (CMOS, 16-bit resolution, first-order ΔΣ loop)

• Multi-Stage Noise Shaping (MASH) incremental ADC (two first-order ΔΣ loops)

• 22-bit incremental ADC (third-order ΔΣ loops, 0.3 mW power consumption)

• Wideband applications (low OSR, 7th-order MASH)
Incremental ADC – Commercial ADCs

Sometimes referred to as charge-balancing ΔΣ ADCs, one-shot ΔΣ ADCs or no-latency ΔΣ ADCs.

- **AD77xx product family, Analog Devices**
  16-bit ~ 24-bit resolution, 1~10 channels, 60~2.5M SPS

- **ADS124x product family, Burr-Brown (Texas Instruments)**
  24-bit resolution, 4~8 channels, 15 SPS

- **CS55xx product family, Cirrus Logic**
  24-bit resolution, 6.25~3840 SPS

- **LTC24xx product family, Linear Technology**
  16-bit ~ 24-bit resolution, 1~16 channels, 6.9~8000 SPS
Low-Distortion Third-Order Structure (1)

Only quantization noise \( Q(z) \) propagates through the integrators.

\[
|v_3(k)| \leq V_{\text{ref}}
\]

\[
Y(z) = U(z) + (1 - z^{-1})^L Q(z)
\]

\[
U(z) - Y(z) = -(1 - z^{-1})^L Q(z)
\]

Low-Distortion Third-Order Structure (2)

\[ u - \frac{3 \cdot 2}{M(M-1)(M-2)} \sum_{m=0}^{M-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_{out}[k]V_{ref} \leq \frac{3 \cdot 2 \cdot V_{ref}}{bc_1c_2M(M-1)(M-2)} \]

\[ D = \frac{3 \cdot 2}{M(M-1)(M-2)} \sum_{m=0}^{M-1} \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_{out}[k]V_{ref} \]

\[ |e| = |u - D| \leq \frac{3 \cdot 2 \cdot V_{ref}}{bc_1c_2M(M-1)(M-2)} \]

Offset Correction in Integrators (1)

Offset Correction in Integrators (2)

Fractal sequencing: a generalization of chopper stabilization. For a cascade of integrators, chopping is inadequate: the integrator outputs for 1 mV offset are 1,-1,1,-1 -> 1,0,1,0 -> 1,1,2,2, etc.

Change the first opamp input/output polarity according to fractal sequencing

\[ S_1 = (+ -) \]
\[ S_2 = (S_1 \bar{S}_1) = ((+ -)(- +)) \]
\[ ... \]
\[ S_n = (S_{n-1} \bar{S}_{n-1}) \]

If \( S_n \) is used for an \( n \)-th order modulator, and the modulator runs for \( M \) clock periods (where \( M/2^n \) is an integer) the first opamp offset will be cancelled in all integrator outputs!!!

Multiplexed Incremental ADC

ADC may be shared between $N$ channels. The FIR decimation filter need not be reset. A low-distortion modulator with FIR NTF needs no reset either.
Optimization of Incremental ADC

\[ v(n) = [stf'(k) \ast u(k) + stf'(k) \ast t(k) + ntf'(k) \ast q(k)]_{M,n} \]

\(v(n)\) is the single output value obtained in the \(n\)th conversion cycle
\(u(k)\) is the input signal
\(t(k)\) is the input-referred thermal noise
\(q(k)\) is the quantization noise
\(stf'(k)\) is the impulse response of the overall signal transfer function \(STF(z)H(z)\)
\(ntf'(k)\) is the impulse response of the overall noise transfer function \(NTF(z)H(z)\)
\(H(z)\) is the transfer function of the decimation filter

Both \(stf'(k)\) and \(ntf'(k)\) have finite lengths (length=\(M\)), where \(M\) is the number of clock periods in each conversion cycle.

Noise Optimization in Incremental ADC

To minimize the overall output noise power, find \( h \) from

\[
\min_\mathbf{h} \quad \mathbf{v}_n^2 = \mathbf{h}^T \cdot \mathbf{O} \cdot \mathbf{h},
\]

where

\[
\mathbf{O} = \frac{5kT}{C_{in}} \mathbf{S}^T \mathbf{S} + \frac{\Delta^2}{6} \mathbf{N}^T \mathbf{N}
\]

\( \mathbf{S} \) and \( \mathbf{N} \) are matrices constructed from the \( \text{stf}(k) \) and \( \text{ntf}(k) \) sequences. They do not contain \( h(n) \).

The problem can be formulated as quadratic programming, or solved analytically for the optimum \( h(n) \) using Lagrange multiplier method. The digital filter is FIR; it can be realized simply as a single multiply-accumulate block.

Two-Channel ADC for a Biopotential Sensor

<table>
<thead>
<tr>
<th>Technology</th>
<th>IBM 90nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Operating Clock</td>
<td>1MHz</td>
</tr>
<tr>
<td>Signal Bandwidth</td>
<td>1k Hz</td>
</tr>
<tr>
<td>No. of multiplexed input channels</td>
<td>2</td>
</tr>
<tr>
<td>Nyquist-Rate</td>
<td></td>
</tr>
<tr>
<td>Data Conversion Rate</td>
<td>2 ksample/sec</td>
</tr>
<tr>
<td>Oversampling Ratio</td>
<td>256</td>
</tr>
<tr>
<td>0dB full-scale voltage</td>
<td>1.2V single-ended</td>
</tr>
<tr>
<td>Max. Input Signal</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.5V_{pp} single-ended</td>
</tr>
<tr>
<td></td>
<td>1.0V_{pp}, fully-differential</td>
</tr>
<tr>
<td>SNDR</td>
<td>&gt;74 dB</td>
</tr>
<tr>
<td>Resolution</td>
<td>&gt;12 bit</td>
</tr>
<tr>
<td>Power</td>
<td>87.65 μW</td>
</tr>
</tbody>
</table>

\[
FoM = \frac{Power}{2^{bit} \cdot 2 \cdot BW} = 1.69 \text{ pJ/Conv.}
\]

Noise-coupled low-distortion delta-sigma loop:
Low-Power Opamp Circuit

Total static current is 1.3 uA.
Auto-Zeroing Comparator

- Static current for each preamp is 50 nA.
- Latches draw no static current.
Simulated PSD of $\Delta \Sigma$ Modulator

- **Conditions**
  - IBM 90nm Technology
  - Sampling clock: 1.024MHz
  - OSR: 256
  - Signal frequency: 375 Hz
  - Single-ended amplitude: $V_{pp}=0.5V$
  - Fully-differential ampl.: $V_{pp}=1.0V$

- **SNDR** = 85.1 dB

- ADC in incremental mode is being simulated now.

- **Simulated FoM**
  \[
  \frac{Power}{2^{bit} \cdot 2 \cdot BW} = \frac{87.65 \mu W}{2^{14} \cdot 2 \cdot 2kHz} = 1.69 \text{ pJ / conv.}
  \]
Measured Spectrum

- Frequency [Hz]
- Magnitude [dBFS]

Graph showing measured spectrum with frequency on the x-axis and magnitude in dBFS on the y-axis.
Chip Layout

- 400MHz Radio
- SRAM
- System CPU
- Digital Filters
- Incremental ADCs
- ADC 1
- ADC 2
- Non-Contact Frontend Amplifier

Dimensions: 2mm x 2mm
Performance Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>IBM 90nm</td>
</tr>
<tr>
<td>• Sampling Frequency</td>
<td>1MHz</td>
</tr>
<tr>
<td>Number of channels</td>
<td>2</td>
</tr>
<tr>
<td>OSR</td>
<td>256</td>
</tr>
<tr>
<td>Signal bandwidth</td>
<td>977Hz/channel</td>
</tr>
<tr>
<td>Oversampling ratio</td>
<td>256</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>73.5 dB</td>
</tr>
<tr>
<td>Maximum input Range</td>
<td>$1V_{pp}$ differential</td>
</tr>
<tr>
<td>Power consumption of the ΔΣ Modulator</td>
<td>13.5 $\mu$W</td>
</tr>
<tr>
<td></td>
<td>Analog: 7.8 $\mu$W / Digital: 5.7 $\mu$W</td>
</tr>
<tr>
<td>Estimated power of digital filter</td>
<td>0.5 $\mu$W</td>
</tr>
<tr>
<td>Area</td>
<td>200µm × 300µm</td>
</tr>
</tbody>
</table>
MUXed Incremental ADC (W. Yu, CICC 2010)

Specifications
- Multiple channels ($N = 20$)
- Narrow bandwidth ($f_B = 3$ kHz)
- SNDR (100 dB)

Design Procedure
- Maximum conversion time for one channel: $T_w = 1/(2Nf_B) = 8.33$ µs
- Maximum number of samples in one conversion cycle: $M_{max} = T_wf_c = 250$
- Modulator design:
  \[
  NTF = \frac{(z-1)^3}{(z-0.5701)(z^2 - 1.39z + 0.6149)}
  \]
System Design (Cont.)

- Noise budget: 90% thermal noise and 10% quantization noise
- Total noise allowed: \( P_{tot} = 10^{-10} \text{ V}^2 \) (100 dB SNR for 1 V\(^2\) output power)
- Estimation of the minimum \( MC_{in} \)
  \( P_t \leq 0.9 \ P_{tot} \quad MC_{in} \geq 460 \text{ pF} \)
- Choose \( M = 230 \) and \( C_{in} = 2 \text{ pF} \)
- Decimation filter optimization

Matlab Simulation

Conversion error versus DC input voltage. Note the absence of tones!
Matlab Simulation

SQNR versus input amplitude for 507 Hz sine-wave input

Peak SQNR = 114 dB
DR = 111 dB
Die Micrograph

INT1

DWA Buffer

INT2

INT3

Adder

Decoupling Caps
The spectrum of the modulator output when the modulator is running as a single sampling ΔΣ modulator with a −2.5 dBFS sine wave input.

ΔΣ modulator mode
SNR = 86.8 dB
SNDR = 83.0 dB
OSR = 230
$f_s = 10$ MHz
power consumption:
6.6 mW (total)
3.8 mW (analog)
2.8 mW (digital)
Measurement Results (Cont’d)

The spectrum of the incremental ADC output (after decimation) with optimal decimation filter (blue line) and with traditional cascaded integrator decimation filter (red line) for a −3.4 dBFS sine wave input.

**Incremental mode**
- **optimal decimation filter**
  - SNR = 83.7 dB
  - SNDR = 81.5 dB
- **cascaded integrator filter**
  - SNR = 82.3 dB
  - SNDR = 79.7 dB

**OSR = 230**

**$f_s = 10$ MHz**

*Power consumption:*
- 6.6 mW (total)
- 3.8 mW (analog)
- 2.8 mW (digital)
The spectrum of the modulator output (continuously-running single sampling ΔΣ modulator) before (red line) and after digital compensation (blue line). The DWA was turned off.

ΔΣ modulator mode:
before digital correction
SNR = 80.1 dB
SNDR = 73.4 dB

after digital correction
SNR = 71.3 dB
SNDR = 63.6 dB
OSR = 230

$f_s = 10$ MHz

Power consumption:
6.6 mW (total)
3.8 mW (analog)
2.8 mW (digital)
ADC with Extended Range [1]

Features of extended-range ADC:

1. Incremental $\Delta\Sigma$ modulator operates at oversampled frequency $f_s$.
2. Feedforward topology is used to lower the signal swings.
3. The 2nd stage ADC converts the residual error at the 1st stage output.
4. The 2nd stage may use a SAR ADC, with an operating frequency $f_s/M$. 
Operation of Extended-Counting ADC

- After M cycles, \( v_2(M) \) becomes
  \[
  v_2(M) = a_1 \cdot a_2 \cdot \frac{M(M-1)}{2} \cdot v_{in} + a_1 \cdot a_2 \cdot V_{ref} \cdot \sum_{j=1}^{M} (M-j) \cdot Y(j)
  \]
  \( v_2(M) \) is converted by the 2\textsuperscript{nd} ADC and combined with the triangularly-weighted output sequence.

- The overall quantization error is ideally only the quantization error of the SAR ADC:
  \[
  E_{Q-ADC} = \frac{2}{a_1 \cdot a_2 \cdot M \cdot (M-1)} E_{Q-SAR}
  \]
Circuit Implementation [1]

SAR ADC
- 11-bit resolution
- dual-capacitor array to reduce the total input capacitance to 3 pF, using a unit cap 48 fF
- Conversion in 11 cycles of charge redistribution.

Incremental $\Delta\Sigma$ Modulator
- Clock frequency = 45.2 MHz.
- OSR = 45.
Measured Results

- Signal: -6dB, 110kHz
- peak SNDR is 86.3 dB, SFDR is 97 dB
- ADC achieved 90.1 dB dynamic range.
- 38 mW power dissipation (excluding output drivers), out of which 23 mW is consumed in the 1st opamp, 9 mW in the 2nd opamp, 1 mW in the SAR, less than 5 mW in all digital blocks.
CT IADC for Biosensor

C-to-D IADC for Displacement Sensing

14-Bit Extended-Counting ADC

For 24 Mpixel image sensor.

References on DACs

References


References on ADCs


[12] S.-W. Chen and R. Brodersen, “A 6b 600MS/s 5.3mW asynchronous ADC in 0.12um CMOS”
References on Extended Counting ADCs


